

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

- 1 1. (Currently Amended) A computer system comprising:  
2 a central processing unit (CPU); and  
3 a cache memory, coupled to the CPU, including:  
4 a main cache having a plurality of cache lines, each of the plurality of  
5 cache lines being that are compressible to form compressed cache lines to store  
6 additional data; and  
7 a plurality of storage pools to hold a segment of the additional data for a  
8 compressed cache line one or more of the plurality of cache lines that are to be  
9 compressed.  
  
1 2. (Original) The computer system of claim 1 wherein each of the plurality of  
2 storage pools include a plurality of fixed width storage fields.  
  
1 3. (Original) The computer system of claim 1 wherein the plurality of cache  
2 lines are included within a plurality of sets.  
  
1 4. (Original) The computer system of claim 3 wherein a storage pool is  
2 allocated to each of the plurality of sets.

1 5. (Original) The computer system of claim 4 wherein an indicator is associated  
2 with each storage field of a storage pool to indicate a line within one of the plurality of  
3 sets to which a storage field is assigned.

1 6. (Currently Amended) The computer system of claim 3 wherein multiple storage  
2 fields within each storage pool is allocated a line within one of the plurality of sets.

1 7. (Original) The computer system of claim 6 wherein each storage field  
2 mapped to one of the plurality of sets is sorted according to a logical ordering.

1 8. (Original) The computer system of claim 3 wherein a storage pool is shared  
2 by two or more of the plurality of sets.

1 9. (Original) The computer system of claim 8 wherein an indicator is associated  
2 with each line of a storage pool to indicate which of the plurality of sets to which a  
3 storage field is assigned.

1 10. (Original) The computer system of claim 1 further comprising a cache  
2 controller coupled to the cache memory.

1 11. (Original) The computer system of claim 10 wherein the cache controller  
2 accesses the cache lines and storage pools in parallel.

1 12. (Original) The computer system of claim 11 wherein accessing the cache  
2 lines and storage pools in parallel comprises the cache controller simultaneously  
3 dispatching set bits to the cache lines and storage pools.

1 13. (Currently Amended) The computer system of claim 10 ~~11~~ wherein the cache  
2 controller accesses the cache lines and storage pools serially.

1 14. (Original) The computer system of claim 3 wherein a storage pool is shared  
2 by all of the plurality of sets.

1 15. (Currently Amended) A cache memory comprising:  
2 main cache having a plurality of cache lines, each of the plurality of cache  
3 lines being that are compressible to form compressed cache lines to store  
4 additional data; and  
5 a plurality of storage pools to hold a segment of the additional data for a  
6 compressed cache line ~~one or more of the plurality of cache lines that are to be~~  
7 ~~compressed.~~

1 16. (Original) The cache memory of claim 15 wherein each of the plurality of  
2 storage pools include a plurality of fixed width storage fields.

1 17. (Original) The cache memory of claim 15 wherein the plurality of cache lines  
2 are included within a plurality of sets.

1 18. (Original) The cache memory of claim 17 wherein a storage pool is allocated  
2 to each of the plurality of sets.

1 19. (Original) The cache memory of claim 18 wherein an indicator is associated  
2 with each storage field of a storage pool to indicate a line within one of the plurality of  
3 sets to which a storage field is assigned.

1 20. (Original) The cache memory of claim 17 wherein multiple storage fields  
2 within each storage pool is allocated a line within one of the plurality of sets.

1 21. (Original) The cache memory of claim 17 wherein a storage pool is shared by  
2 two or more of the plurality of sets.

1 22. (Original) The cache memory of claim 21 wherein an indicator is associated  
2 with each line of a storage pool to indicate which of the plurality of sets to which a  
3 storage field is assigned.

1 23. (Original) The cache memory of claim 17 wherein a storage pool is shared by  
2 all of the plurality of sets.

1 24. (Currently Amended) A method comprising:  
2 compressing one or more of a plurality of cache lines to form one or more  
3 compressed cache lines store additional data by:  
4 storing a first component of the data in a main cache; and  
5 storing a second component of the data in one or more of a plurality of  
6 storage pools.

1 25. (Original) The method of claim 24 wherein the plurality of cache lines are  
2 included within a plurality of sets.

1 26. (Original) The method of claim 25 further comprising allocating a storage  
2 pool to each of the plurality of sets.

1 27. (Original) The method of claim 26 further comprising associating an  
2 indicator with each storage field of a storage pool to indicate a line within one of the  
3 plurality of sets to which a storage field is assigned.

1 28. (Original) The method of claim 25 further comprising allocating a storage  
2 pool to a line within one of the plurality of sets.

1 29. (Original) The method of claim 28 further comprising mapping each storage  
2 field to one of the plurality of sets.

1 30. (Original) The method of claim 29 further comprising associating an  
2 indicator with each line of a storage pool to indicate which of the plurality of sets to  
3 which a storage field is assigned.

1 31. (Currently Amended) A computer system comprising:  
2 a central processing unit (CPU); and  
3 a cache memory, coupled to the CPU, including:

4 main cache having a plurality of cache lines, each of the plurality of cache  
5 lines being that are compressible to form compressed cache lines to store  
6 additional data; and  
7 a plurality of storage pools to hold a segment of the additional data for a  
8 compressed cache line; one or more of the plurality of cache lines that are to be  
9 compressed and  
10 a main memory device coupled to the CPU.

1 32. (Original) The computer system of claim 31 wherein each of the plurality of  
2 storage pools include a plurality of fixed width storage fields.

1 33. (Original) The computer system of claim 31 wherein the plurality of cache  
2 lines are included within a plurality of sets.